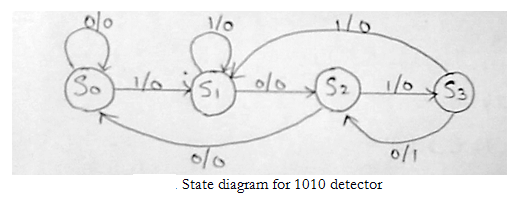
1. **AIM:** To write Verilog Code for any suitable sequence detector and simulate with test bench.

**02 APPARATUS:** Software used Xilinx ISE 13.4

**03 FORMULA: N.A**

**04 THEORY:**

A sequence detector is a sequential state machine it accepts an input a string of bits either 0 or 1. Its output goes to one when a target sequence has been detected. In a Mealy machine, output depends on the present state and the external input (x). Hence in the diagram, the output is written outside the states, along with inputs. The state diagram of a Mealy machine for a 1010 detector is:



The state table for the above diagram:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Present State | Next State | | Out put | |
| X=0 | X=1 | X=0 | X=1 |
| S0 | S0 | S1 | 0 | 0 |
| S1 | S2 | S1 | 0 | 0 |
| S2 | S0 | S3 | 0 | 0 |
| S3 | S2 | S1 | 1 | 1 |

**05 PROCEDURE:**

# Open Xilinx ISE and create a new project. Select path of working project directory and enter name of project. Click on Next

# Select the Family, Device, Package and Speed of Xilinx board and also select your programming language (Verilog/VHDL). Here I am using Verilog language. Click on Next Project summery window occurs. Click on Finish.

# Click on Project > New Source

# Select Source type is Verilog Module and enter the file name and click on Next.

# Define Module Window. Here we can define inputs & outputs and its bit/bus size. Also define clock signal for clocking operation. Click on Next.

# Summery Window then Click on Finish.

# The Project Navigator window will come write the code of the programs in that.

# Double click on synthesize, on the left hand side

# To see the circuit click on view RTL schematic option and then press ok.

# Go on clicking in the black area to zoom in the circuit elements.

# To run simulation, click on Simulation option at the top of left column.

# To create a Test bench, create New Source. Select Verilog Test Fixture

# Template of Test bench will be created instantiating.

# Add the testing code in the initial block below Add Stimulus here comment.

# Double click on Simulate Behavioral Model option.

# This is the simulation window. We can verify the working using waveforms or using printed statements at the bottom.

**06 VERILOG CODE:**

module mealy1010 (inp,clk,rst,y);  
/\*A verilog module for 1010 mealy overlapping FSM \*/

input inp,clk,rst;  
output reg y;  
reg [1:0] current,next;

parameter first = 2’b00,  
second = 2’b01,  
third = 2’b10,  
fourth = 2’b11;  
always @ (posedge clk)  
begin  
if (rst)  
current <= first;  
else  
current <= next;  
end

always @ (current or inp)  
begin  
case (current)  
first: if (inp == 1)  
begin  
next = second;  
y = 0;  
end

else  
begin  
next = current;  
y = 0;  
end  
second: if (inp == 0)  
begin  
next = third;  
y = 0;  
end

else  
begin  
next = current;  
y = 0;  
end  
third: if (inp == 1)  
begin

next = fourth;

y = 0;  
end

else  
begin  
next = first;  
y = 0;  
end

fourth: if (inp == 0)  
begin  
y= 1;  
next = third;  
//y = 1;  
end

else  
begin  
next = second;  
y = 0;  
end

default: next = first;  
end case  
end  
end module

**07 RESULT:** The Verilog Code for 1010 sequence detector is running successfully and providing the correct output.

**08 CONCLUSION:** After performing this experiment we learn how to detect a particular sequence step for Mealy FSM.